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(54) A circuit for controlling the maximum current in a power-MOS transistor used for driving a load connected to ground

Schaltung zur Steuerung des maximalen Stroms in einen Leistungs-MOS-Transistor mit einer Last, die an Masse geschaltet ist

Circuit de contrôle du courant maximal dans un transistor MOS de puissance utilisé pour commander une charge connectée à la masse

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(56) References cited:
EP-A- 0 397 015 **DE-A- 3 536 447**

- **PATENT ABSTRACTS OF JAPAN vol. 13, no. 264 (E-774)19 June 1989**

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D scription

The present invention relates to a circuit for controlling the operation of a MOS power transistor used for driving a load connected to earth, of th kind defined in the preamble of Claim 1.

A known circuit of this kind, disclosed in EP-A-0 397 015, includes means for sensing the voltage across and the current passing through the MOS transistor (MOST) and providing corresponding voltage signals to respective inputs of a first transconductance amplifier stage arranged to produce an output current related to the product of the MOST voltage and current, i.e. related to the MOST power dissipation. Said first amplifier stage is directly supplied by the d.c. operating power supply to which also the MOS transistor is coupled. The output of said first amplifier stage is coupled to one input of a second differential amplifier stage, the output of which is connected to the gate of the MOST. The second amplifier stage has a second input coupled to a reference voltage source and includes a current mirror circuit coupled to a charge pump circuit. The second amplifier stage also includes a bias circuit coupled to an external source of bias voltage. This prior art control circuit is arranged so as to limit the power dissipated in the MOST to a predetermined safe value.

Figure 1 of the appended drawings shows another typical circuit of the prior art used to drive a load L connected to earth GND. This circuit includes a MOS power transistor M1, for example, an n-channel transistor, with its drain connected to a direct-current supply voltage V_S and its source connected to the load. If the load L is inductive, a free-wheeling diode D1 is arranged in parallel therewith in order, each time the transistor M1 is cut off, to dissipate the energy which the load itself has stored during the previous stage in which M1 was conductive.

The transistor M1 is used as a switch and therefore operates in the triode region. In this region, the transistor M1 operates with a low voltage V_{DS} and behaves essentially as a voltage-controlled resistance, the resistance value of which is lower, the greater the quantity by which the gate-source voltage (V_{GS}) exceeds V_{DS} + V_{TH}, where V_{TH} is the threshold voltage of the MOS transistor, that is, a voltage such that the transistor is cut off when V_{GS} is less than V_{TH}.

In the circuit shown in Figure 1, it is of fundamental importance that V_{DS} should be small since the lower this voltage is, the greater is the power supplied to the load L.

The gate of the transistor M1 is driven by a charge pump circuit CP of known type. This circuit enables the gate capacitance of the transistor M1 to be charged to a voltage greater than the supply voltage V_S, although with currents of low intensity.

If the source of M1 is accidentally short-circuited to earth GND or if the resistance of the load L is very small, the transistor M1 no longer operates in the triode region, but operates in a region in which its drain current depends on V_{GS} and is almost independent of V_{DS}.

To limit the power dissipated by the power transistor M1 under these circumstanc s in order to prevent damage, it is necessary to limit the drain current by reducing the gate voltage.

The problems connected with the control of the maximum current in a circuit configuration of the type shown in Figure 1 relate essentially to the frequency stability of the entire system and to the precision of the control.

Figures 2 and 3 of the appended drawings show two different known solutions for controlling the maximum current which can flow through the MOS power transistor M1.

The solution shown in Figure 2 uses an amplifier A which may be a normal operational amplifier or a transconductance operational amplifier. The non-inverting input (+) of this amplifier is connected to the drain of M1 and its inverting input (-) is connected to the negative terminal of a reference-voltage generator V_R, the positive terminal of which is connected to the positive terminal of the supply voltage V_S. The amplifier A also has a supply terminal s which is connected to V_S. The output of the amplifier is connected to the gate of M1.

A resistor R_S is connected between the drain of M1 and the supply voltage V_S.

The current supplied to the gate of M1 by the charge pump CP and the current flowing in the load L are indicated I_{CP} and I_L, respectively.

Figure 3 shows another solution according to the prior art. In Figure 3 the same alphabetical references have again been attributed to parts and elements already described above.

In the solution of Figure 3, the resistor R_S is between the source of M1 and the load L. The reference-voltage generator V_R is between the load and the non-inverting input (+) of the operational amplifier A. The inverting input of the amplifier is connected to the source of M1.

With both the solutions described with reference to Figures 2 and 3, the maximum current which the MOS transistor M1 can supply to the load L is:

$$I_{Lmax} = V_R/R_S$$

The current-regulator circuits of Figures 2 and 3 use operational amplifiers and, in order to operate in a stable manner, must be suitably compensated. The gate capacitance of M1, which, in both cases, is connected to the output of the operational amplifier A, involves the introduction of an additional pole to the frequency response which, with the use of an operational amplifier which itself has to be compensated, may make the system unstable, particularly when the MOS transistor used has large physical dimensions and hence a high gate capacitance.

If the amplifier A of the diagrams of Figures 2 and 3 is a transconductance amplifier, it must have a very high gain g_m in order to enable precise regulation of the

maximum current in the transistor M1 since, in practice, the current I_{CP} coming from the charge pump CP is never known sufficiently accurately.

If the gate capacitance of the MOS transistor M1 is used to compensate the transconductance operational amplifier, the high gain g_m may involve problems of frequency instability, particularly if the MOS transistor used has small dimensions and hence a small gate capacitance.

The object of the present invention is to provide a circuit for controlling the maximum current in a MOS power transistor used for driving a load connected to earth, which enables the current to be controlled more precisely with a low-gain transconductance amplifier which has very good frequency stability characteristics and simple circuitry.

According to the invention, this object is achieved by a control circuit having the features defined in Claim 1.

Further characteristics and advantages of the invention will become clear from the detailed description which follows with reference to the appended drawings, provided purely by way of non-limiting example, in which:

Figure 1, which has already been described, shows a typical circuit according to the prior art, including a MOS power transistor for driving a load connected to earth,

Figures 2 and 3, which have already been described, show two solutions according to the prior art for controlling the maximum current which can flow through a MOS power transistor for driving a load connected to earth,

Figure 4 is a diagram of a control circuit according to the invention, and

Figures 5 and 6 show two possible embodiments of the circuit of Figure 4, in greater detail.

The control circuit of Figure 4 differs from that described above with reference to Figure 3 in that the output of the charge pump CP is connected to the supply terminal s of the operational amplifier A rather than to the gate of the power transistor M1. In particular, this amplifier is a transconductance amplifier with a fairly small gain g_m.

In spite of the low value of g_m, the current regulation which can be achieved by the circuit of Figure 4 is quite precise. In fact, in the circuit of Figure 4, the current is not regulated according to a sum of currents at the gate of M1, as in the case of the circuits of Figures 2 and 3, but the output of the amplifier A itself charges or discharges the gate capacitance of M1.

In this layout, the gate capacitance of the MOS power transistor M1 is also used to stabilise the circuit for controlling the current supplied to the load. The low gain g_m of the transconductanc amplifier A m ans that the circuit as a whole is stable although the dimensions of the transistor M1 are small.

With reference to Figure 5, in a first embodiment, the transconductance amplifier A is formed as a current-mirror circuit and includes two branch circuits each including a respective pair of complementary transistors.

In particular, one branch of the current-mirror circuit has two transistors Q1 and Q3 which, in the embodiment illustrated in particular, are bipolar transistors of the pnp type and the npn type, respectively.

The other branch of the current-mirror circuit also includes a pair of transistors Q2 and Q4, of the pnp and npn types, respectively.

The emitters of the transistors Q1 and Q2 are connected to the output of the charge pump CP, their bases are connected to each other, and their collectors are connected to the collectors of Q3 and Q4, respectively. The bases of Q3 and Q4 are connected to each other and their emitters are connected to the source of M1 and to the positive pole of the reference-voltage generator V_R, respectively.

The base of each of the transistors Q2 and Q3 is connected to its emitter so that it can operate essentially as a diode.

The transistors Q1-Q4 are formed so that Q1 and Q2 have the same emitter area and Q3 and Q4 have the same emitter area.

The collector of Q4 (Q2) represents the output of the entire transconductance amplifier A and is connected to the gate of M1.

The current supplied to the gate of M1 by the amplifier A is indicated I_G.

In operation, the MOS power transistor M1 can supply the load L with a maximum current when I_G is zero, the maximum current depending upon the resistance of the resistor R_S and upon the reference voltage V_R:

$$I_{Lmax} = V_R/R_S.$$

In practice, the gain of the transconductance amplifier A of Figure 5 is the gain g_m of the transistors Q3 and Q4 and is low since the current I_{CP} is very small.

The gate capacitance of M1 is sufficient for the frequency compensation even if the area of the transistor is fairly small.

Figure 6 shows an embodiment of the circuit according to the invention which is similar to that described above with reference to Figure 5, from which it differs, as can easily be seen, in that the reference-voltage generator VR is absent.

In the embodiment of Figure 6, the reference voltage is not provided by a generator outside the transconductance amplifier A but is produced within the amplifier because the emitter area of at least one of the transistors Q2 and Q3 differs from that of the respective tran-

sistor Q1 or Q4. In general, if the emitter areas of Q2 and Q3 are assumed to be m and n tim s those of Q1 and Q4, respectively, this produces a r ference voltage:

$$V_R = V_T \ln (m\ n)$$

in which V_T is the equivalent-temperature voltage and ln indicates the natural logarithm.

The maximum current which the MOS power transistor M1 can supply to the load L is thus expressed by:

$$I_{Lmax} = V_R/R_S = [\ln (m\ n)]\ V_T/R_S.$$

The equation given above indicates how, in the circuit of Fig. 6, the limit value of the current which can be supplied to the load can be defined by different emitter areas of one or both of the transistors Q2 and Q3 which operate essentially as diodes.

The solutions described above with reference to Figures 5 and 6 provide for the use of bipolar transistors to form the transconductance amplifier. It will be clear to an expert in the art, however, that the amplifier could also be formed with CMOS transistors.

Moreover, the foregoing, which relates to an n-channel MOS power transistor, naturally also applies to a p-channel MOS transistor, with the necessary alteration of details.

The main advantages of the control circuit according to the invention are essentially as follows.

The desired frequency stability can be achieved without the need to add compensating capacitors since the gate capacitance of the MOS power transistor, which may even be small (a MOS power transistor of small dimensions), can be used for this purpose because stability is in any case ensured by the low value of the gain g_m of the transconductance amplifier A.

With a low-gain transconductance amplifier, it is also possible to achieve very precise control of the current supplied to the load since the output of the transconductance amplifier regulates the gate voltage of the transistor M1 directly, unlike the circuits of the prior art in which the gate is charged with a current represented by the sum of the current coming from the charge pump (the value of which cannot, in practice, be determined precisely) and the current coming from the transconductance amplifier. The current-control circuit according to the invention is also quite simple and a small number of components is needed to form the transconductance amplifier. This means that it can easily be used in monolithic integrated circuits.

The use of a transconductance amplifier does not adversely affect the R_{DSon} of the MOS power transistor under non-current-limitation conditions. In operation, the transconductance amplifier absorbs hardly any current from the charge pump CP, enabling the gate voltage of M1 to reach the value it would reach in the absence of the circuit for controlling the maximum current supplied to the load, and the R_{DSon} is therefore the same as it would be if the gate of M1 were supplied directly by the charge pump CP without the amplifier A.

Naturally, the principle of the invention remaining the same, the forms of embodiment and details of construction may be varied widely with respect to. those described and illustrated purely by way of non-limiting example, without thereby departing from the scope of the present invention as defined in the appended Claims.

Claims

1. A circuit for controlling the operation of a MOS power transistor (M1) used for driving a load (L) connected to earth (GND), including:

   a direct-current voltage supply (V_S) to which the drain of the MOS transistor (M1) is connected,

   a resistor (R_S) in series with the drain-source path of the MOS transistor (M1),

   a charge pump circuit (CP) for enabling the gate capacitance of the MOS transistor (M1) to be charged to a voltage higher than the supply voltage (V_S), and

   transconductance amplifier means (A) having the output connected to the gate of the MOS transistor (M1), a supply terminal(s) connected to the output of the charge pump circuit (CP) and the inputs (+, -) connected to said resistor (R_S);

   characterised in that said resistor (R_S) is connected between the source of the MOS transistor (M1) and the load (L); the said transconductance amplifier means comprising a single stage transconductance operational amplifier (A) having a first input connected to the source of the MOS transistor (M1) and a second input coupled to the load (L); said single stage transconductance operational amplifier (A) being arranged so as to limit the maximum current (I_{LMAX}) in the MOS transistor (M1) to a value proportional to a predetermined reference voltage (V_R).

2. A control circuit according to Claim 1, characterised in that it includes a reference voltage generator (V_R) which is outside the transconductance operational amplifier (A) and is connected between a terminal of the resistor (R_S) and an input (+) of the amplifier (A).

3. A control circuit according to Claim 2, characterised in that the transconductance operational amplifier

(A) includes a current-mirror circuit (Figure 5) comprising:

a first branch circuit including two complementary transistors (Q1, Q3) between the output of the charge pump circuit (CP) and a terminal of the resistor (R_S), and

a second branch circuit, also including two complementary transistors (Q2, Q4), between the output of the charge pump circuit (CP) and the reference voltage generator (V_R).

4. A control circuit according to Claim 3, characterised in that the transconductance operational amplifier (A) includes a current-mirror circuit (Figure 6) comprising:

first and second branch circuits (Q1, Q3; Q2, Q4) which are disposed between the output of the charge pump circuit (CP) and respective terminals of the resistor (R_S), and each of which includes two complementary transistors (Q1, Q3; Q2, Q4) of which one (Q3; Q2) has its base (gate) connected to its collector (drain) so that it can operate essentially as a diode,

at least one of the transistors (Q3; Q2) which can operate as diodes having an emitter (source) area larger than those of the other transistors (Q1; Q4) of the current-mirror circuit.

Patentansprüche

1. Schaltkreis zur Steuerung der Arbeitsweise eines MOS-Leistungstransistors (M1), der zum Ansteuern einer Last (L) verwendet wird, die mit Masse (GND) verbunden ist, wobei der Schaltkreis aufweist:

eine Gleichspannungsquelle (V_S), mit der die Senke des MOS-Transistors (M1) verbunden ist,
einen Widerstand (R_S), der mit der Senken/Quellen-Strecke des MOS-Transistors (M1) in Serie liegt,
eine Ladungspumpstufe (CP), um die Kapazität der Steuerelektrode des MOS-Transistors (M1) auf eine Spannung laden zu können, die über der Quellenspannung (V_S) liegt, und
einen Steilheitsverstärker (A), dessen Ausgang mit der Steuerelektrode des MOS-Transistors (M1) verbunden ist, dessen Ansteueranschluß (Ansteueranschlüsse) am Ausgang der Ladungspumpstufe (CP) liegt (liegen) und dessen Eingänge (+, -) mit dem Widerstand (R_S) verbunden sind;

dadurch gekennz ichnet, daß der Widerstand (R_S) zwischen der Quelle des MOS-Transistors (M1) und der Last (L) liegt; der Steilheitsverstärker einen einstufigen Steilheits-Operationsverstärker (A) mit einem ersten Eingang, der mit der Quelle des MOS-Transistors (M1) verbunden ist, und mit einem zweiten Eingang enthält, der mit der Last (L) verbunden ist; der einstufige Steilheits-Operationsverstärker (A) so aufgebaut ist, daß er den maximalen Strom (I_{LMAX}) im MOS-Transistor (M1) auf einen Wert begrenzt, der proportional einer vorgegebenen Bezugsspannung (V_R) ist.

2. Steuerschaltkreis gemäß Anspruch 1, **dadurch gekennzeichnet,** daß er einen Bezugsspannungsgenerator (V_R) aufweist, der außerhalb des Steilheits-Operationsverstärkers (A) angeordnet ist und zwischen einem Anschluß des Widerstands (R_S) und einem Eingang (+) des Verstärkers (A) liegt.

3. Steuerschaltkreis gemäß Anspruch 2, **dadurch gekennzeichnet,** daß der Steilheits-Operationsverstärker (A) eine Stromspiegelschaltung (Fig. 5) aufweist, die enthält:

einen ersten Schaltkreiszweig, der zwischen dem Ausgang der Ladungspumpstufe (CP) und einem Anschluß des Widerstands (R_S) liegt und zwei komplementäre Transistoren (Q1, Q3) aufweist, und
einen zweiten Schaltkreiszweig, der zwischen dem Ausgang der Ladungspumpstufe (CP) und dem Bezugsspannungsgenerator (V_R) liegt und gleichfalls zwei komplementäre Transistoren (Q2, Q4) aufweist.

4. Steuerschaltkreis gemäß Anspruch 3, **dadurch gekennzeichnet,** daß der Steilheits-Operationsverstärker (A) eine Stromspiegelschaltung (Fig. 6) aufweist, die enthält:

einen ersten und zweiten Schaltkreiszweig (Q1, Q3; Q2, Q4), die zwischen dem Ausgang der Ladungspumpstufe (CP) und entsprechenden Anschlüssen des Widerstands (R_S) liegen, wobei jeder Schaltkreiszweig zwei komplementäre Transistoren (Q1, Q3; Q2, Q4) aufweist, von denen einer (Q3; Q2) mit seiner Basis (Steuerelektrode) an seinem Kollektor (Senke) liegt, so daß er im wesentlichen als Diode arbeiten kann,
zumindest einer der Transistoren (Q3; Q2), der als Diode arbeiten kann, eine Emitter-(Quellen)-Zone besitzt, die größer als die der anderen Transistoren (Q1; Q4) der Stromspiegelschaltung ist.

R v ndicati ns

1. Circuit pour commander le fonctionnement d'un transistor de puissance MOS (M1) utilisé pour attaquer une charge (L) connectée à la masse (GND), comprenant :

une source de tension d'alimentation continue (V_S) à laquelle le drain du transistor MOS (M1) est connecté,
une résistance (R_S) en série avec le trajet drain-source du transistor MOS (M1),
un circuit de pompe à charge (CP) pour permettre à la capacité de grille du transistor MOS (M1) d'être chargée jusqu'à une tension supérieure à la tension d'alimentation (V_S), et
un moyen formant amplificateur transconducteur (A) ayant la sortie connectée à la grille du transistor MOS (M1), une(des) borne(s) d'alimentation connectée(s) à la sortie du circuit de pompe à charge (CP) et les entrées (+, -) connectées à ladite résistance (R_S) ;

caractérisé en ce que ladite résistance (R_S) est connectée entre la source du transistor MOS (M1) et la charge (L) ; ledit moyen formant amplificateur transconducteur comprenant un amplificateur transconducteur opérationnel à un étage (A) ayant une première entrée connectée à la source du transistor MOS (M1) et une seconde entrée connectée à la charge (L) ; ledit amplificateur transconducteur opérationnel à un étage (A) étant disposé de manière à limiter le courant maximal (I_{LMAX}) dans le transistor MOS (M1) à une valeur proportionnelle à une tension de référence prédéterminée (V_R).

2. Circuit de commande selon la revendication 1, caractérisé en ce qu'il comprend un générateur de tension de référence (V_R) qui est extérieur à l'amplificateur transconducteur opérationnel (A) et qui est connecté entre une borne de la résistance (R_S) et une entrée (+) de l'amplificateur (A).

3. Circuit de commande selon la revendication 2, caractérisé en ce que l'amplificateur transconducteur opérationnel (A) comprend un circuit de miroir de courant (figure 5) contenant :

une première branche de circuit comprenant deux transistors complémentaires (Q1, Q3) entre la sortie du circuit de pompe à charge (CP) et une borne de la résistance (R_S), et
une seconde branche de circuit, comprenant également deux transistors complémentaires (Q2, Q4), entre la sortie du circuit de pompe charge (CP) et le générateur de tension de référence (V_R).

4. Circuit de commande selon la revendication 3, caractérisé en ce que l'amplificateur transconducteur opérationnel (A) compr nd un circuit de miroir de courant (figure 6) contenant :

des première et seconde branches de circuit (Q1, Q3 ; Q2, Q4) qui sont disposés entre la sortie du circuit de pompe à charge (CP) et des bornes respectives de la résistance (R_S), et qui comprennent chacune deux transistors complémentaires (Q1, Q3 ; Q2, Q4) dont un (Q3 ; Q2) a sa base (grille) connectée à son collecteur (drain) de sorte qu'il peut fonctionner essentiellement comme une diode,
au moins un des transistors (Q3 ; Q2) qui peuvent fonctionner comme des diodes ayant une zone d'émission (source) plus grande que celles des autres transistors (Q1 ; Q4) du circuit de miroir de courant.

FIG. 1 *PRIOR ART*

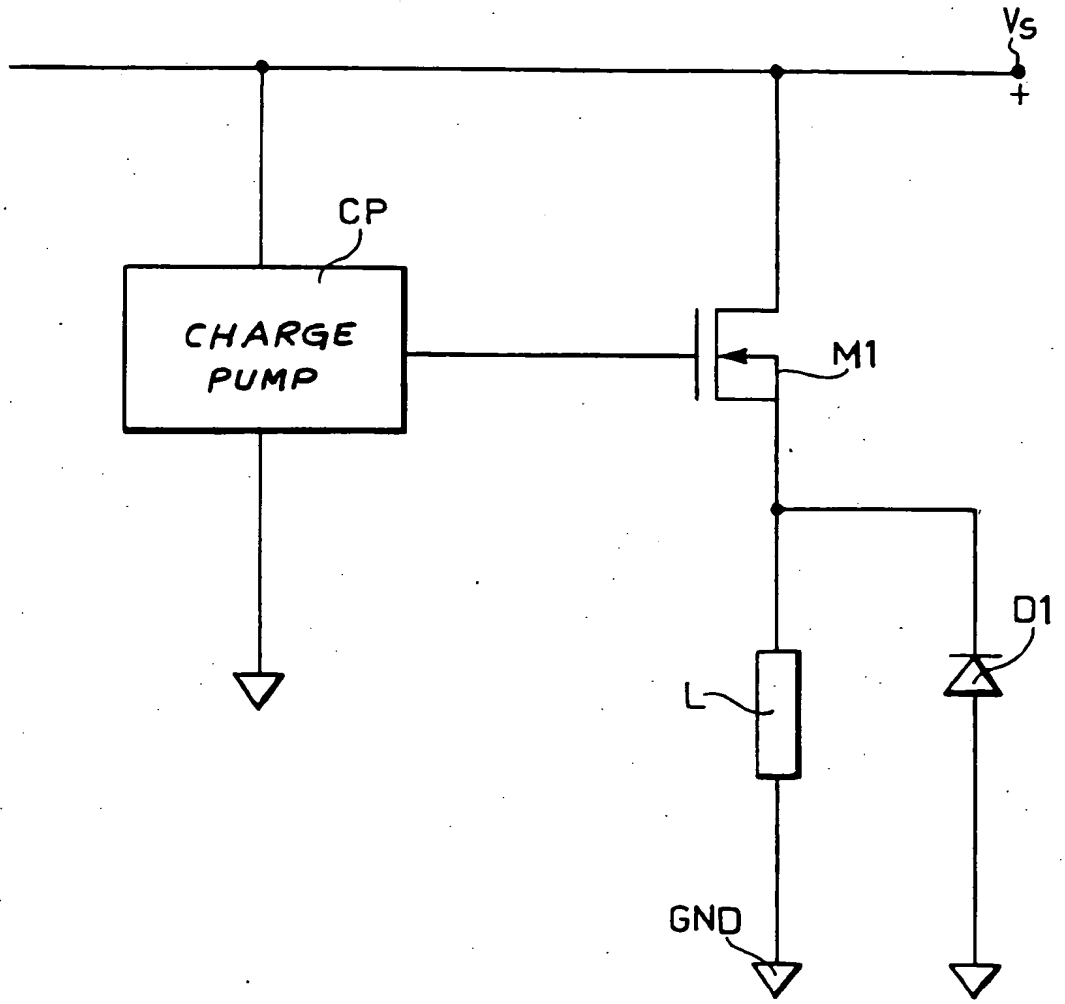

FIG. 2 PRIOR ART

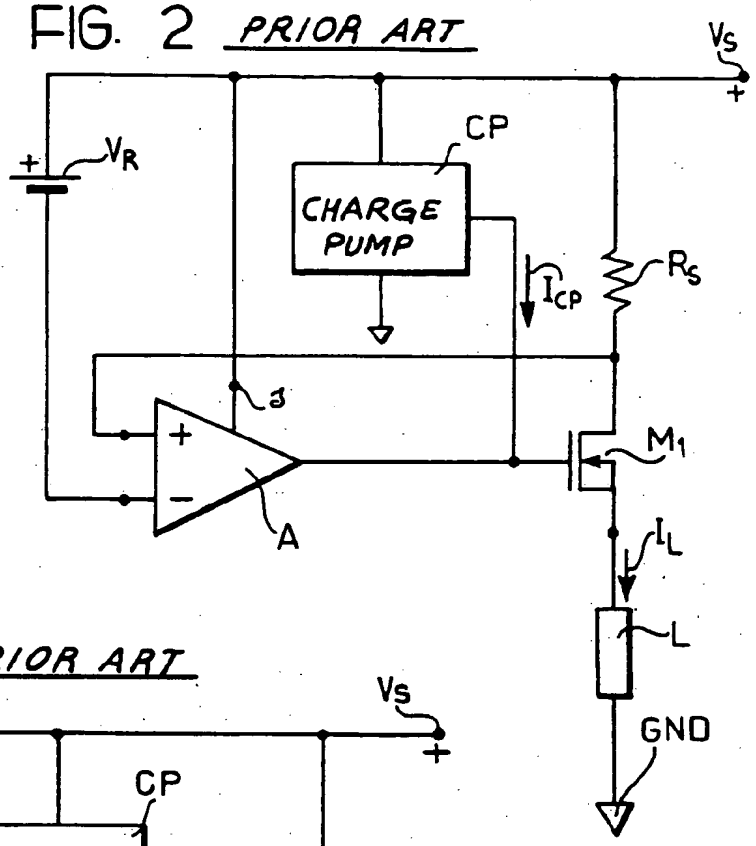

FIG. 3 PRIOR ART

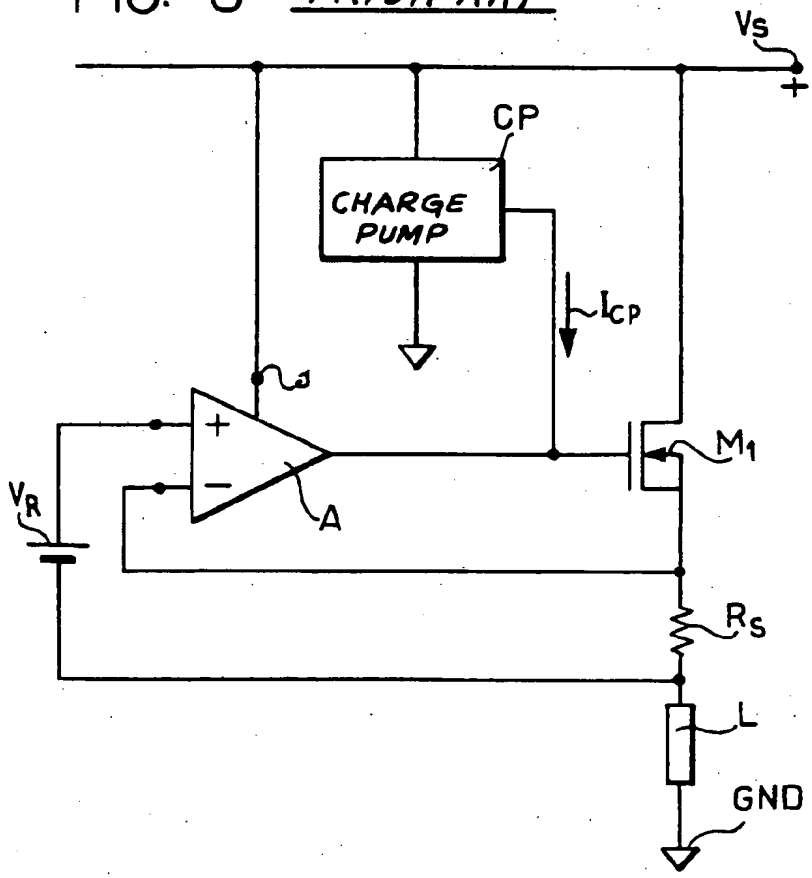

FIG. 4

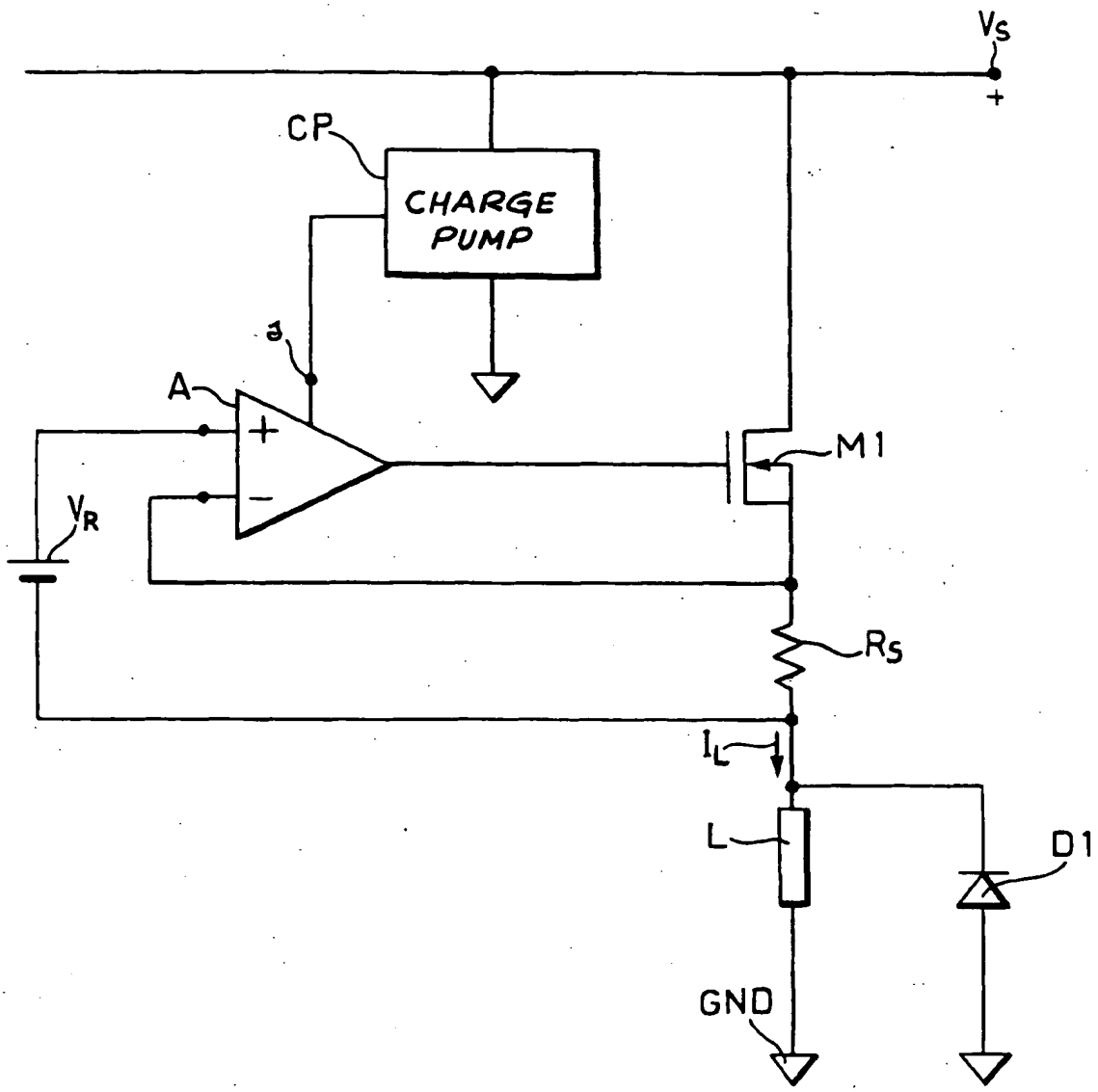

FIG. 5

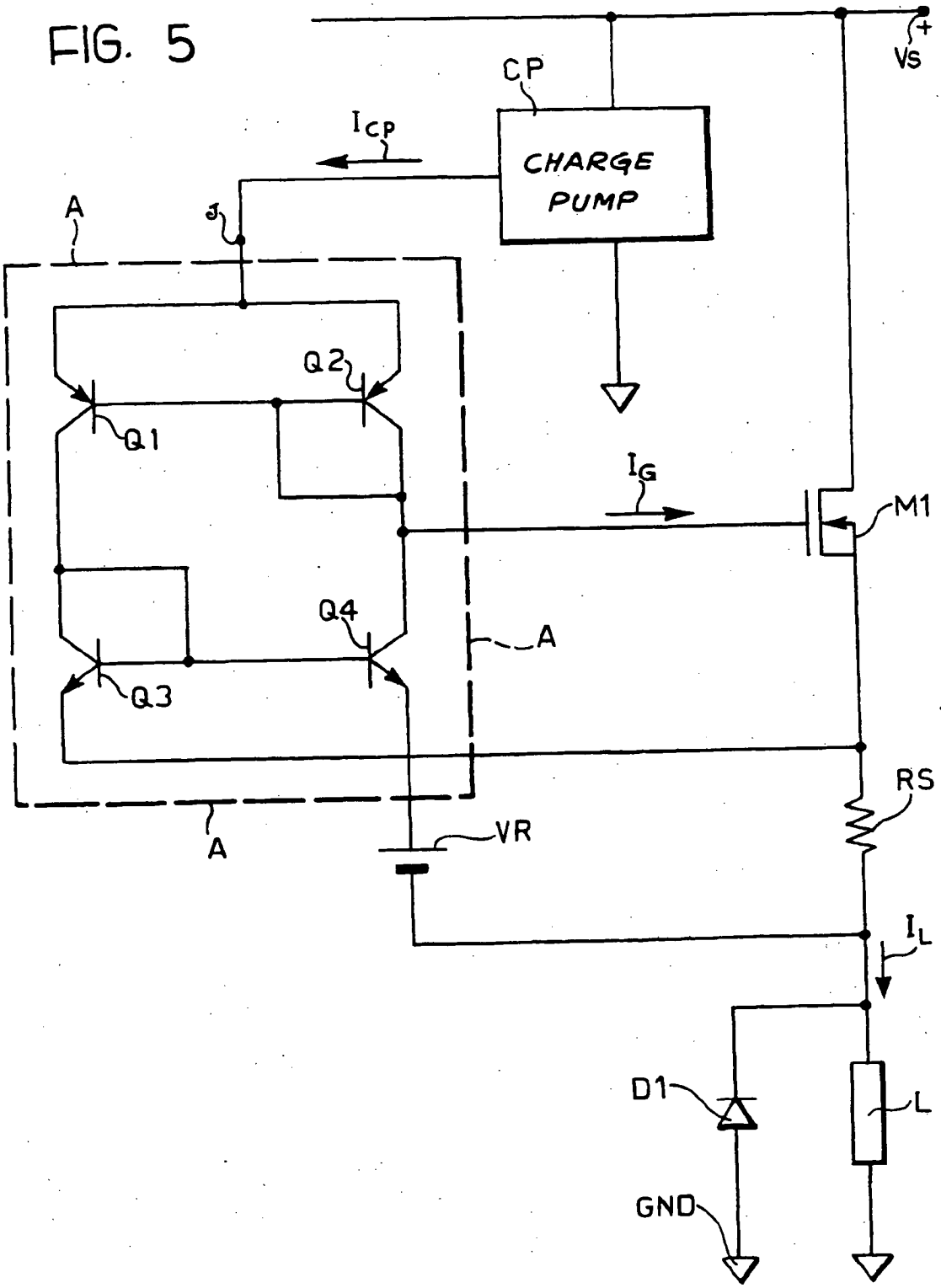

FIG. 6